REMARKS

This Amendment is responsive to the Final Office Action mailed on February 16, 2006, and is accompanied by a Request for Continued Examination. No new matter has been added.

I. Objection to Claim 14

Claim 14 has been amended to correct the typographical error identified by the Examiner.

II Rejection of Claims 15 and 20 under Section 112

Claims 15 and 20 have been revised to remove the phrases identified by the Examiner as lacking antecedent basis.

III. Obviousness Rejections of Independent Claims

For the reasons set forth below, Applicants respectfully submit that the independent claims are patentably distinct from the cited references, and request that the obviousness rejections of the claims be withdrawn.

Independent Claim 1

The Examiner rejected Claim 1 on obviousness grounds over the background of the invention (BOI) section of the present application in view of U.S. Pat. 6,065,097 to Feierbach et al. ("Feierbach"). Applicants respectfully submit that this rejection is improper because the BOI section and Feierbach do not individually or collectively teach or suggest the following limitations of the claim: "subsequent to retrieving the cache tag from the cache memory bank into the microprocessor, retrieving the cache data associated with the memory read request from the cache memory bank into the microprocessor."

The Examiner points to Feierbach in connection with these limitations, citing col. 4, lines 39-55 and Fig. 5. In Feierbach, however, the retrieval of the cache data occurs in parallel with, and thus not subsequent to, the retrieval of the cache tag. This is apparent from Figure 5 of Feierbach, which shows the cache tag being retrieved over the "E$ Tag" lines while the corresponding cache data is being retrieved over the "Data" lines. This is in contrast to Applicants' preferred embodiments, in which the cache tag is retrieved before the cache data, and in which both are retrieved over the same set of bus lines. See present application at, e.g., page 9, line 20 to page 10, line 2, and Fig. 7, SysAD lines. An important benefit of this feature is that it enables the microprocessor's pin count to be reduced, as a common set of pins can be used to

retrieve both the cache tag and the cache data. Thus, the manufacturing cost of the microprocessor can be significantly reduced.

As best understood by Applicants, the Examiner is construing the above-quoted claim language as covering the scenario shown in Figure 5 of Feierbach, in which the cache tag and cache data are retrieved in parallel but the cache tag transfer completes before the cache data transfer. To the extent this may be the Examiner's position, Applicants respectfully submit it is improper. Nevertheless, Applicants have amended Claim 1 to clarify that the claim does not cover this scenario. Specifically, Applicants have amended the claim to clarify that the retrieval of the cache data (i.e., the transfer of cache data on the bus from the cache memory bank to the microprocessor) does not overlap in time with the retrieval of the cache tag.

Applicants also respectfully submit that the rejection of Claim 1 is improper because the Examiner has not identified a teaching, suggestion or motivation to combine Feierbach with Figure 4 of the BOI section. In connection with this issue, the Examiner asserts that one would have been motivated to add the teachings of Feierbach to Fig. 4 of the BOI section for the following reason: "In doing so, if a tag match occurs, then a cache hit exists and data already retrieved from the cache memory into the microprocessor can be processed. Therefore, the data latency reduces and the overall performance of the microprocessor increases." The Examiner thus appears to assert that performance would be increased if the cache tag comparison function of the L2 Cache Tag Element in Fig. 4 were moved to the microprocessor as in Feierbach. The Examiner has not shown, however, that Feierbach's method of performing the cache tag comparison inside the microprocessor would enable the microprocessor to detect the cache hit any earlier in the cache-data retrieval process. (Note that the cited portion of Feierbach does not claim such a performance benefit, but merely indicates that the cache data being retrieved can be processed, as opposed to being discarded.) Thus, the Examiner has not shown that the alleged performance benefit could even be realized, let alone recognized by one skilled in the art. Thus, the Examiner has not identified a valid motivation to combine Feierbach with Figure 4 of the BOI section.

For the foregoing reasons, Applicants request that the Examiner withdraw the rejection of Claim 1.

Independent Claim 8

The Examiner rejected Claim 8 on obviousness grounds over the BOI section of the present application in view of Feierbach. Applicants respectfully submit that this rejection is improper because the BOI section and Feierbach do not individually or collectively teach or suggest the following limitations: "wherein the microprocessor is configured to retrieve a cache tag from the bank of general purpose random access memory before retrieving corresponding cache data from the bank of general purpose random access memory." In this regard, Applicants submit that this language does not cover the scenario shown in Figure 5 of Feierbach, in which the cache tag transfer is completed before the cache data transfer is completed.

To further distinguish Claim 8 from Feierbach, Applicants have amended the claim to state that the microprocessor "is configured to retrieve the cache tag and the corresponding cache data from the bank of general purpose random access memory over a common set of bus lines." This is in contrast to Feierbach, in which separate bus lines, and thus separate microprocessor pins, are used to retrieve the cache tag and cache data from the external memory. See Figs. 3 and 5 of Feierbach.

Applicants also respectfully submit that the rejection of Claim 8 is improper because, as set forth above, the Examiner has not identified a teaching, suggestion or motivation to combine Feierbach with Figure 4 of the BOI section.

In view of the foregoing, Applicants submit that Claim 8 is patentably distinct from the BOI section and Feierbach.

Independent Claim 13

As with Claims 1 and 8, the Examiner rejected Claim 13 on obviousness grounds over the BOI section in view of Feierbach. Applicants respectfully submit that this rejection is improper because the BOI section and Feierbach do not individually or collectively teach or suggest the following limitations: "an address transformation circuit that translates the memory address supplied by the central processing unit into a first address for retrieving a cache tag from an external cache memory, and into a second address for retrieving cache data from the external cache memory. In connection with these limitations, the Examiner relies on Figure 4 of the BOI section of the present application, taking the position that the cache index generated by the

microprocessor represents both the "first address" and the "second address" recited in the claim. Applicants respectfully submit that this interpretation is improper.

Applicants also respectfully submit that the rejection of Claim 13 is improper because the BOI section and Feierbach do not teach or suggest that "the microprocessor is configured to use the first address to retrieve the cache tag from the external cache memory, and to then use the second address to retrieve the cache data from the external cache memory." The Office Action does not address these limitations of the claim.

Applicants also respectfully submit that the rejection of Claim 13 is improper because, as set forth above for Claim 1, the Examiner has not identified a teaching, suggestion or motivation to combine Feierbach with Figure 4 of the BOI section.

Dependent Claims

Many of the dependent claims recite limitations that provide additional patentable distinctions over the cited references. As one example, Claim 4 recites "comparing the cache tag to the memory address within a system controller device that interfaces the microprocessor to a main memory." In connection with these limitations, the Examiner points to Fig. 4 of the present application. In the prior art design shown in Figure 4, however, the cache tag comparison is performed by the cache tag memory (labeled "Level 2 Cache Tag Element"), and not the system control device. See present application at page 4, lines 20-30. Thus, the Examiner's reliance on Figure 4 is misplaced.

As another example, Claim 5 states that "the method comprises mapping the memory address into a cache tag address and a cache data address that are sequentially provided to the cache memory bank to retrieve the cache tag and the cache data therefrom." In connection with these limitations, the Examiner states that the feature recited in Claim 5 is "similar" to the feature described in the BOI section in which the level 2 cache (Figure 4) compares a microprocessor-supplied memory address to data stored in the level 2 cache. Applicants respectfully disagree, and submit that the Examiner has not shown how or why the limitations of Claim 5 are suggested. Although the Examiner also cites page 6, line 20 to page 7, line 3 of the BOI section, it is not clear from the Office Action how the Examiner is relying on this disclosure.

As another example, Claim 6 recites "wherein mapping the memory address comprises using an address mapping function that subdivides a memory space of the cache memory bank

into separate cache tag locations and cache data locations." In connection with these limitations, the Examiner relies on Figure 4 of the BOI section, noting that the cache tag and cache data are stored in separate memory elements and locations. In the design shown in Figure 4, however, the same address (cache index) is passed to the cache data element and the cache tag element. Thus, the design shown in Figure 4 does not use "an address mapping function that subdivides a memory space of the cache memory bank into separate cache tag locations and cache data locations."

Other patentable distinctions are recited in other dependent claims, including the new dependent claims added by this amendment.

IV. New Claims 28-35

New Claims 28-35 are directed to aspects of the system controller shown in the embodiment of Figure 6 and described, e.g., at page 7, lines 22-24; page 11, lines 3-31, and page 14, lines 20-29 of the present application. As none of the art of record suggests a system controller capable of performing its own cache tag comparison, these claims are believed to be patentably distinct from the art of record.

V. Conclusion

In view of the foregoing amendments and remarks, Applicants submit that the application is in condition for allowance. If any issues remain which can potentially be resolved by telephone, the Examiner is invited to call the undersigned attorney of record at his direct dial number listed below.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 5-8-06

By: 

Ronald J. Schoenbaum
Registration No. 38,297
Customer No. 20,995
(949) 721-2950

2396223\dns
022306